

[illegible][illegible][illegible][illegible]

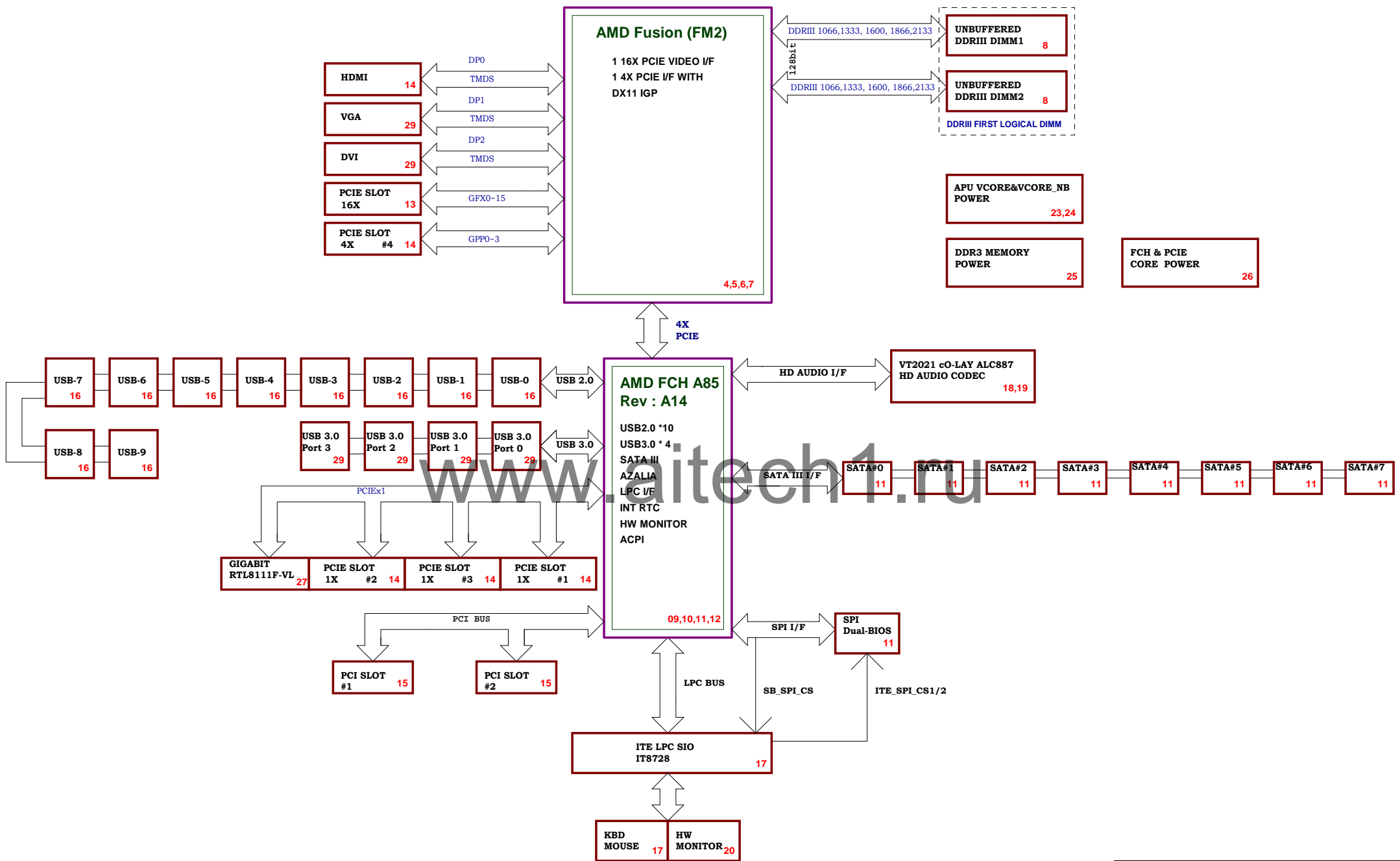
## Component value change history

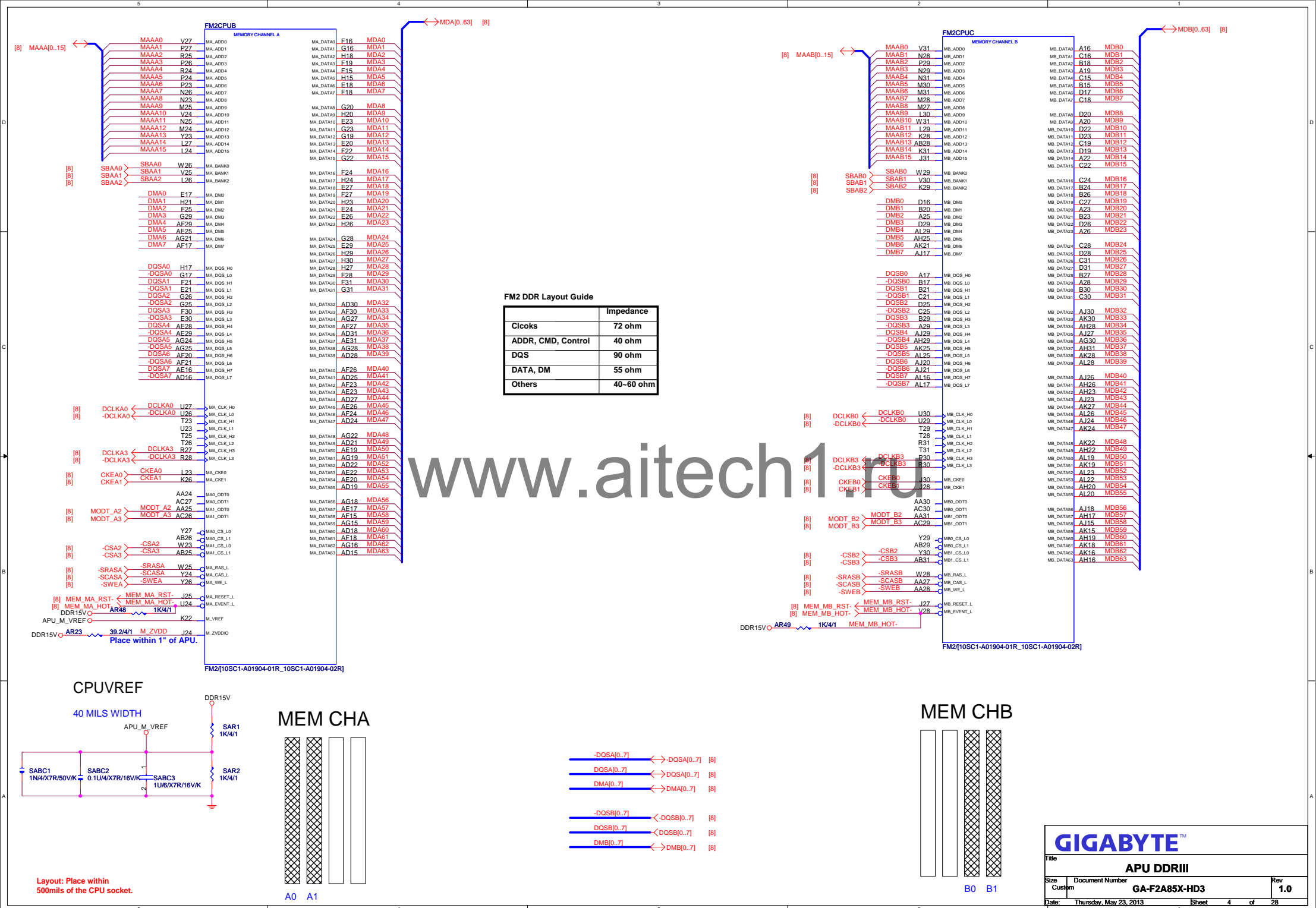
**P-Code : U13016-0**  
**Tip/Top : F285XH3**

[illegible]

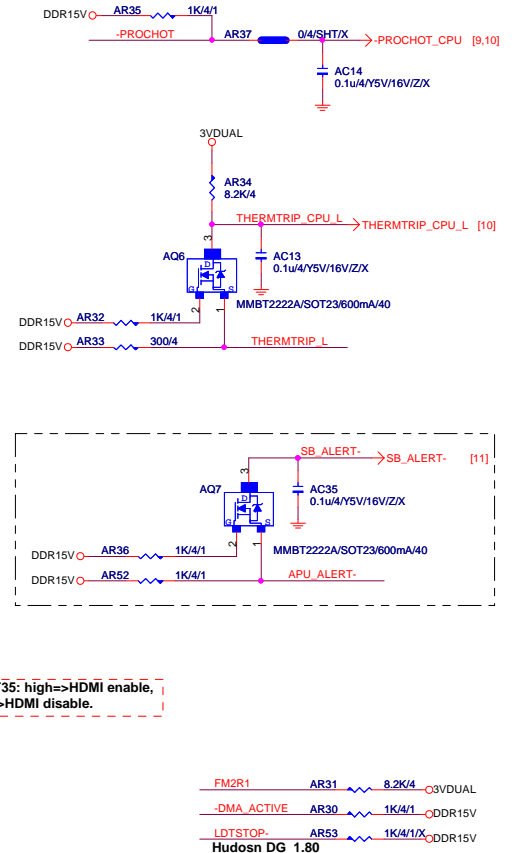
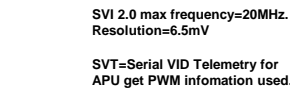
### Circuit or PCB layout change for next version

[illegible]



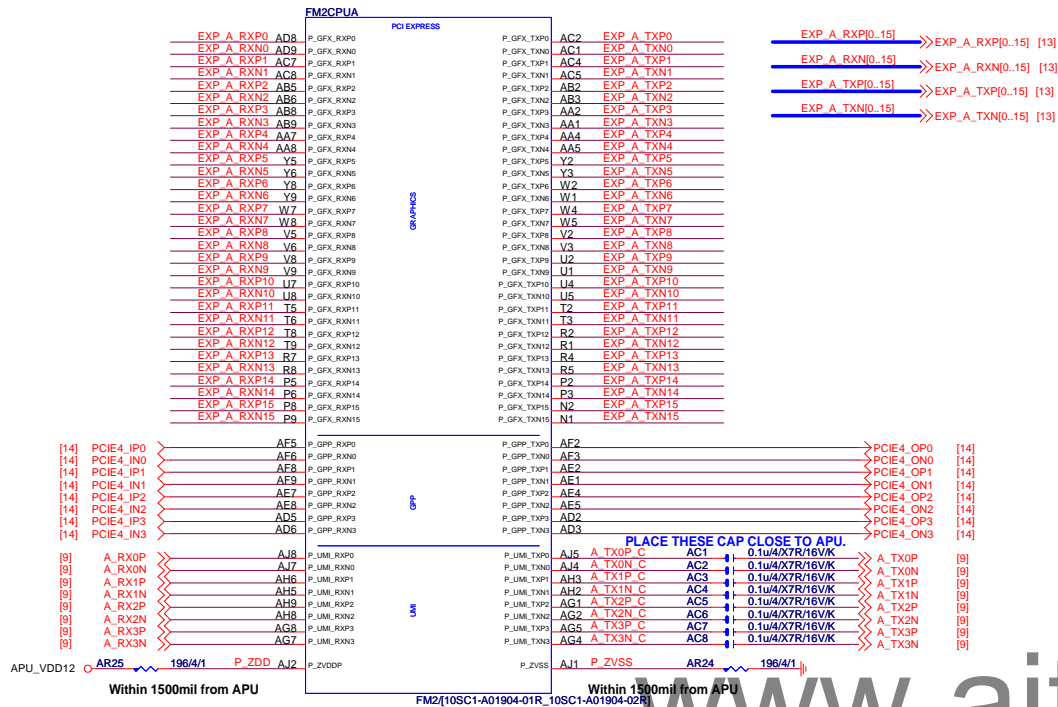






	APU FM2
Group A	VDDA25:1.8~2.7V/0.5A
Group A	DDR15V:0.8~2.3V/30A
Group B	VCORE: 0.8~2.0V/120A
Group B	VCORE_NB:1.2V/50A
Group B	VDDP:1.2V/5A
Group B	VDDR:1.2V/5A

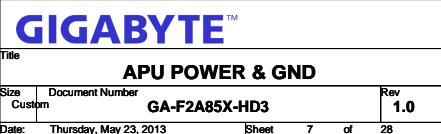
**Group A must early than Group B**



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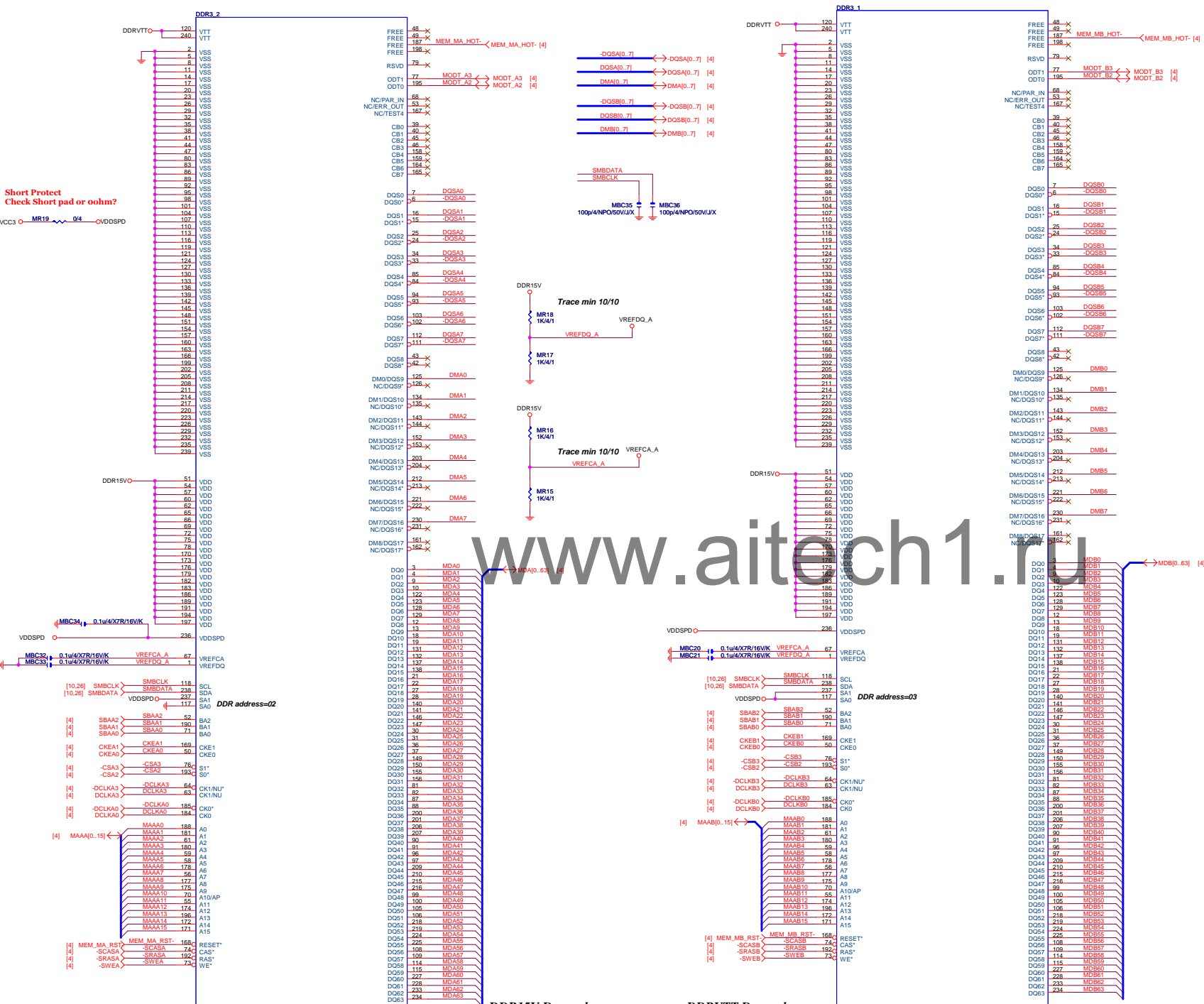
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Title			APU GFX, GPP, SB I/F		
Size	Document Number	Rev			
Custom	GA-F2A85X-HD3	1.0			
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Short Protect  
Check Short pad or oohm?

VCC3 MR19 04 CVDSPD



DDR3240BKVAD

DDR15V Decouple

DDRVT Decouple

DDR3240BKVAD

Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

DDR15V

DDRVT

GIGABYTE

Title: DDR III CHANNEL A

Size: Custom

Document Number: GA-F2A85X-HD3

Date: Thursday, May 23, 2013

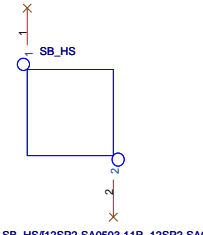
Sheet: 8 of 28

Rev: 1.0



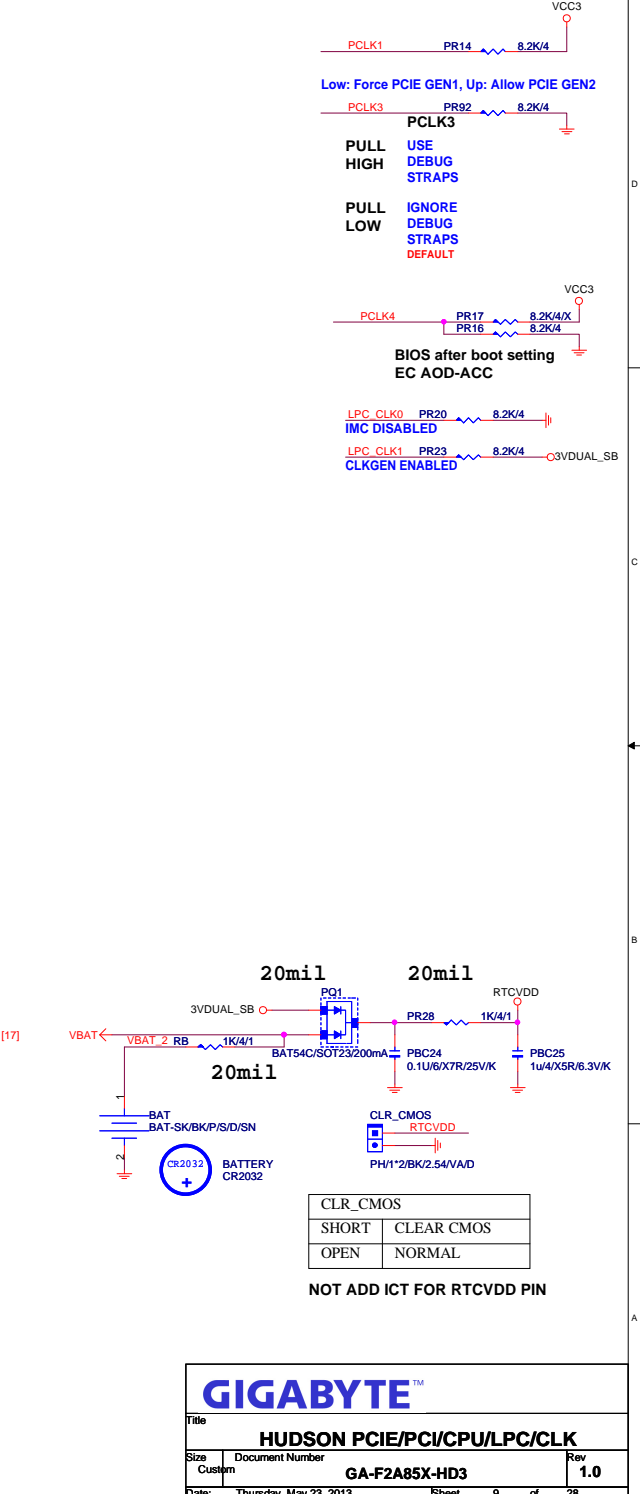
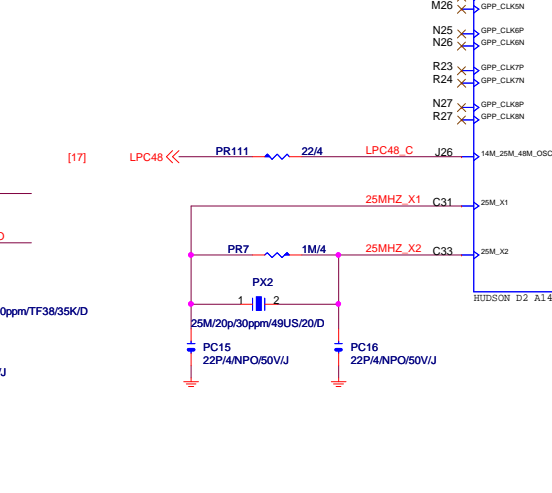
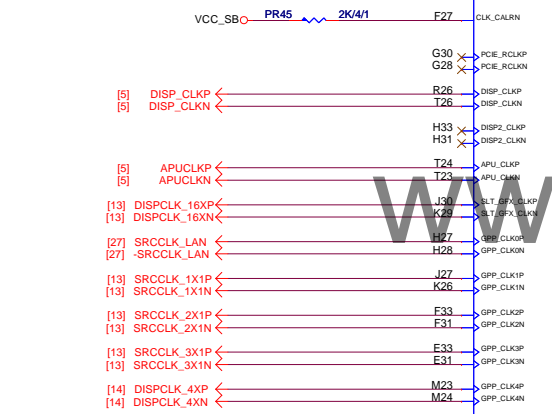
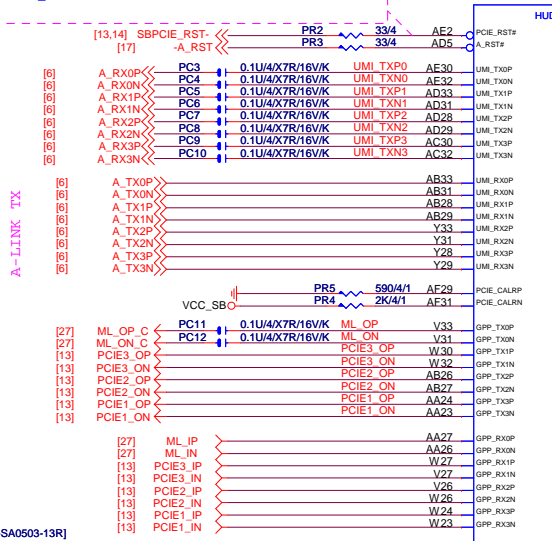
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

## S.B HEATSINK



SB\_HS[12SP2-SA0503-11R\_12SP2-SA0503-12R\_12SP2-SA0503-13R]  
SB\_HS 12SP2-SA0503-1\*R by ECU A11

## PCIE\_RST# connect to APU PCIe Devices/Slots

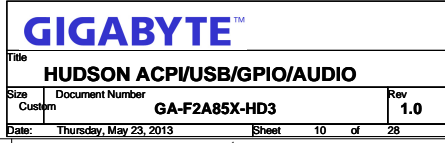


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HUDSON PCIe/PCI/CPU/LPC/CLK

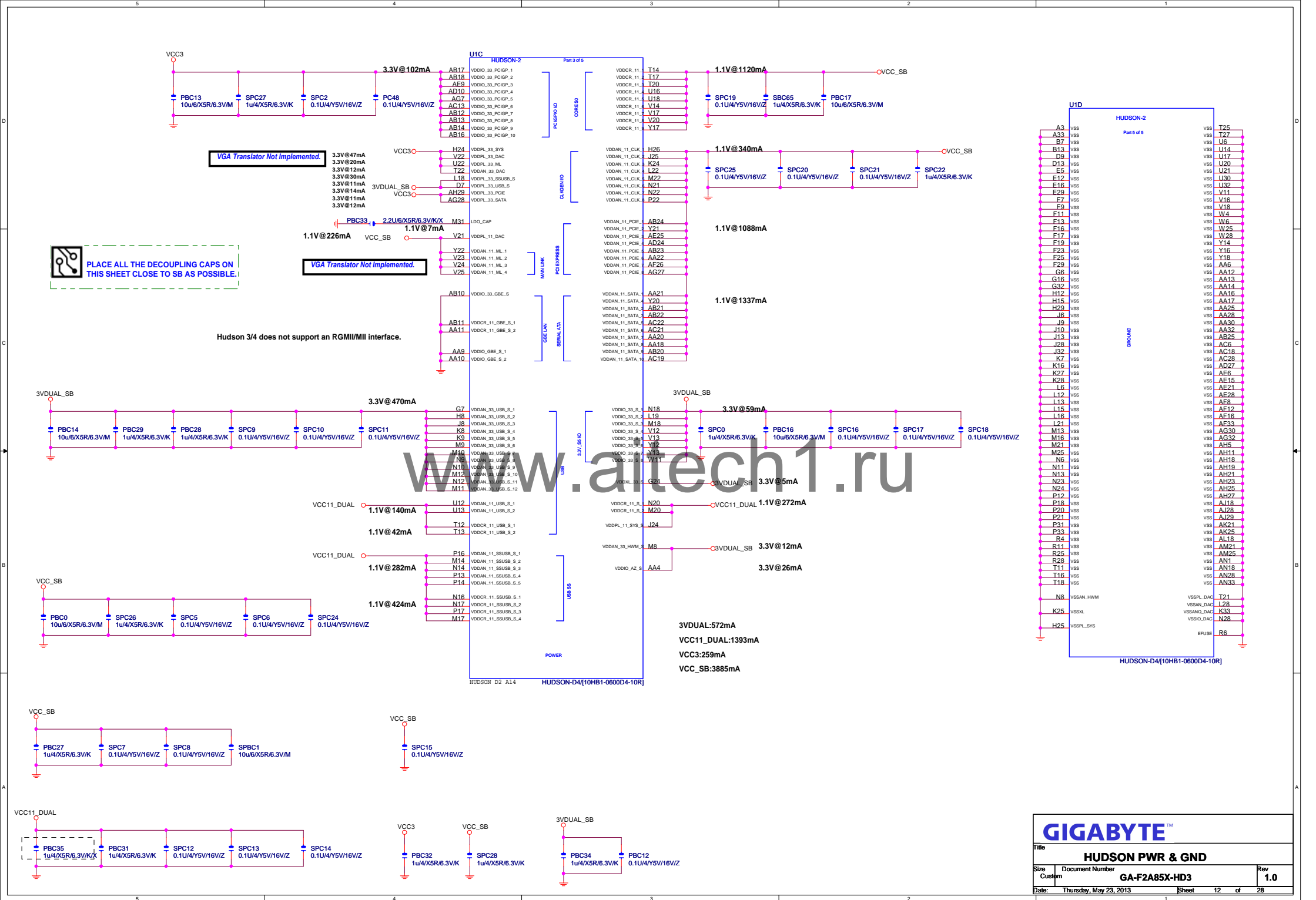
Title	Customer	Document Number	Rev
		GA-F2A85X-HD3	1.0

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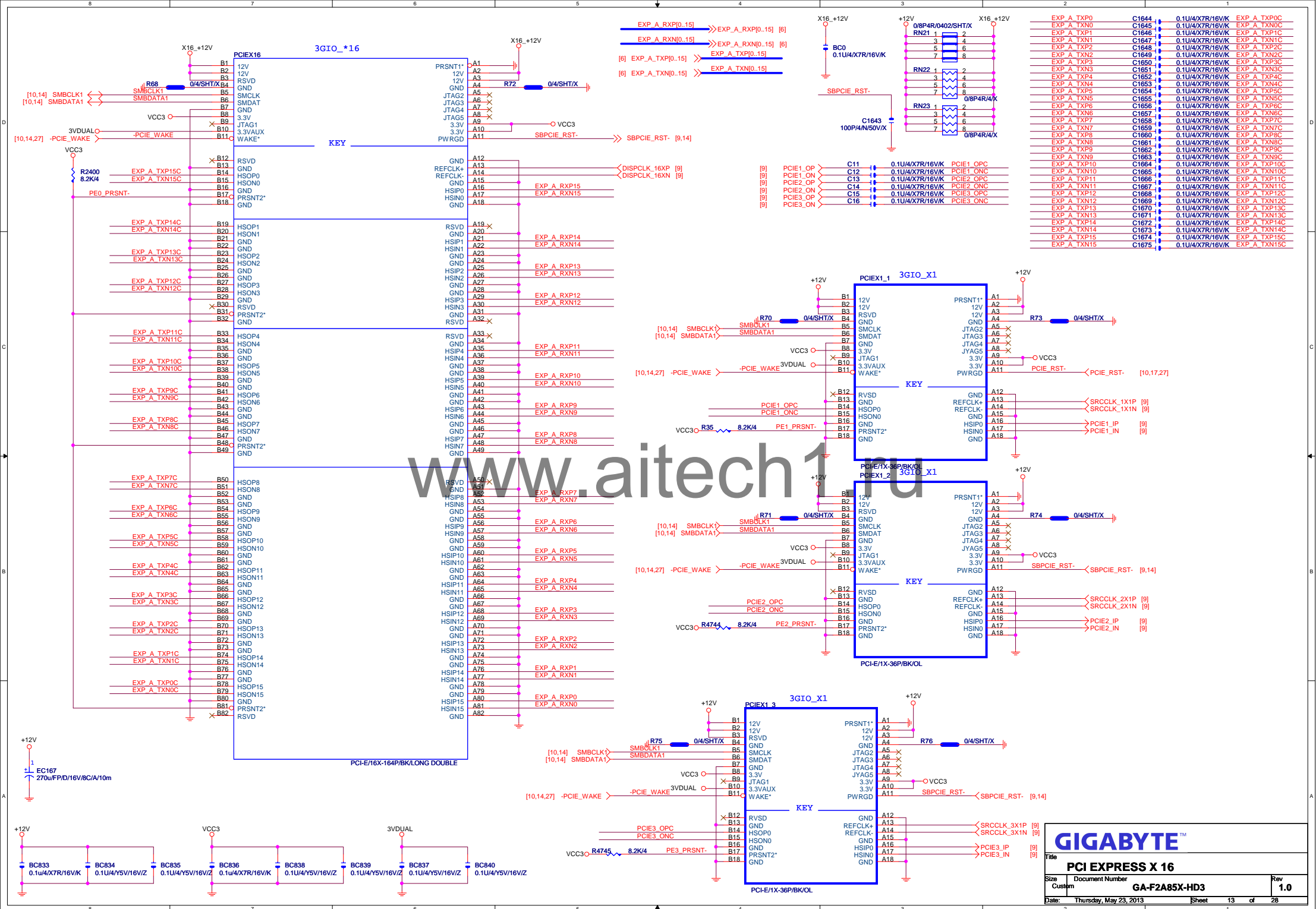


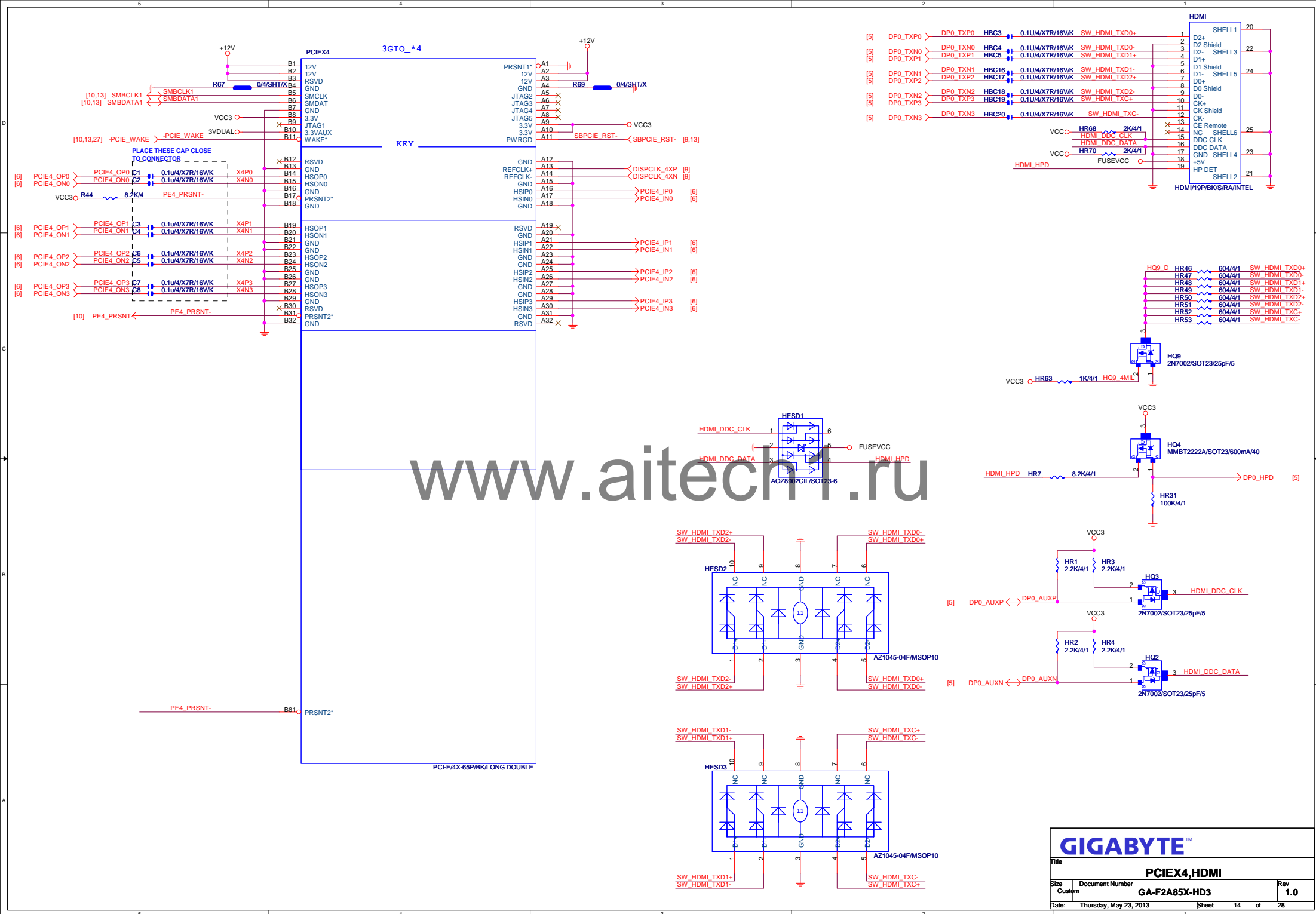




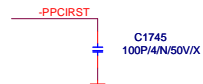
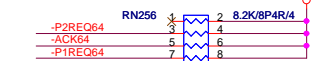
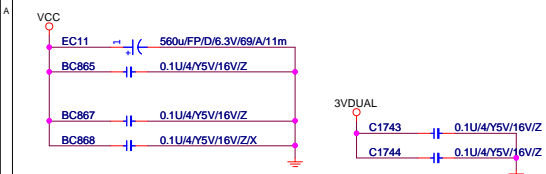
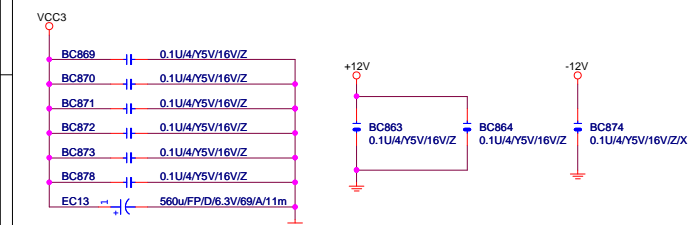
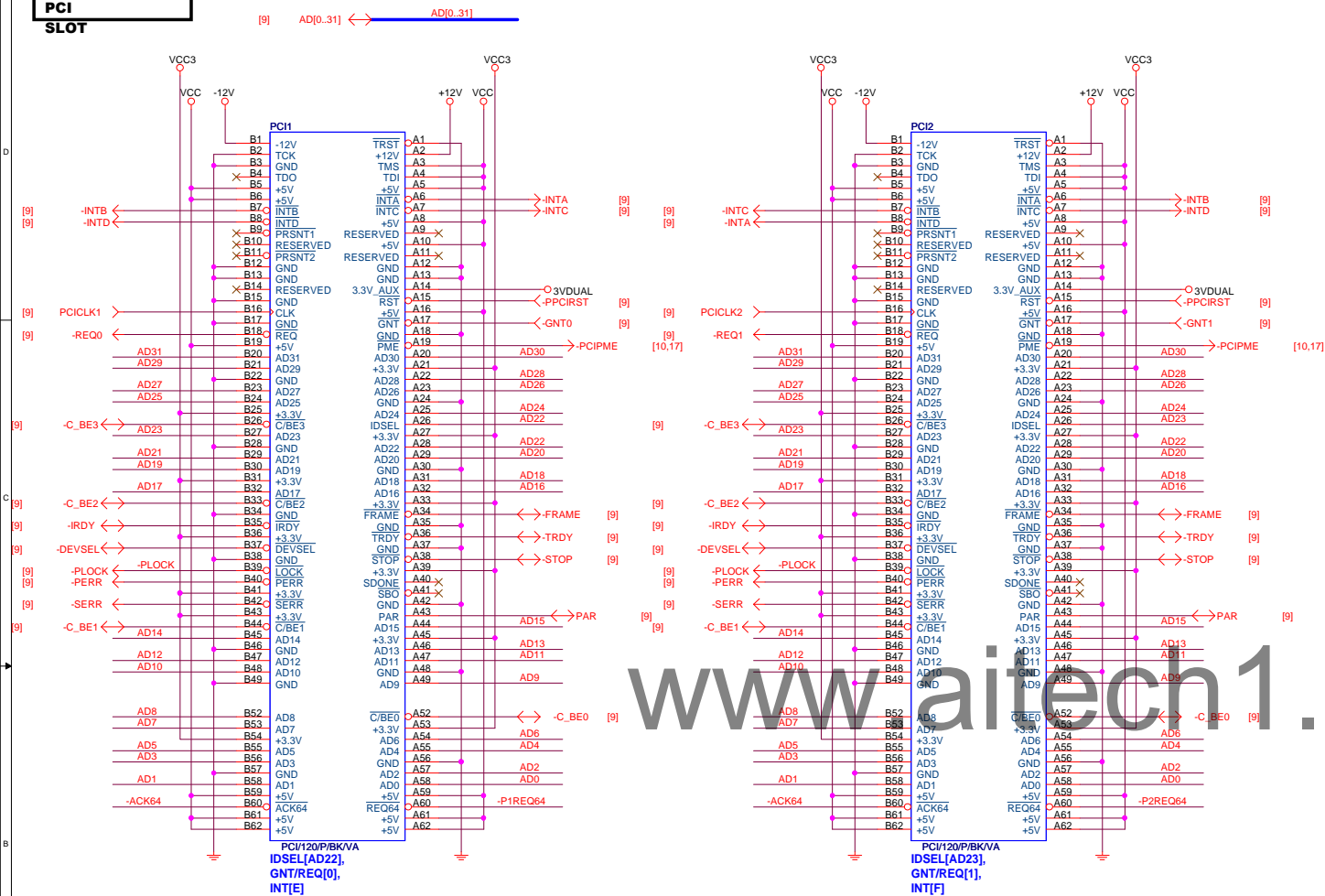


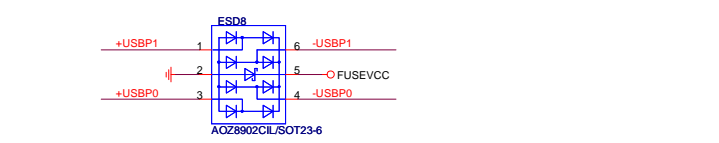
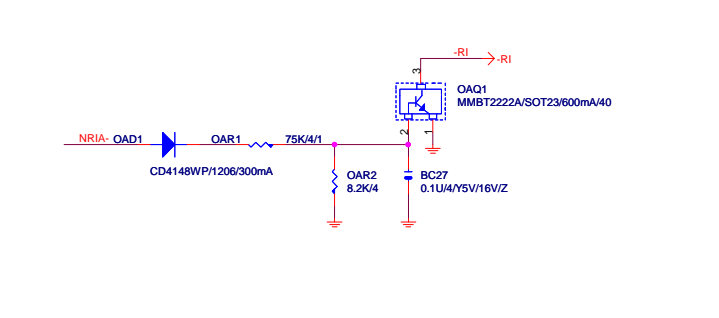


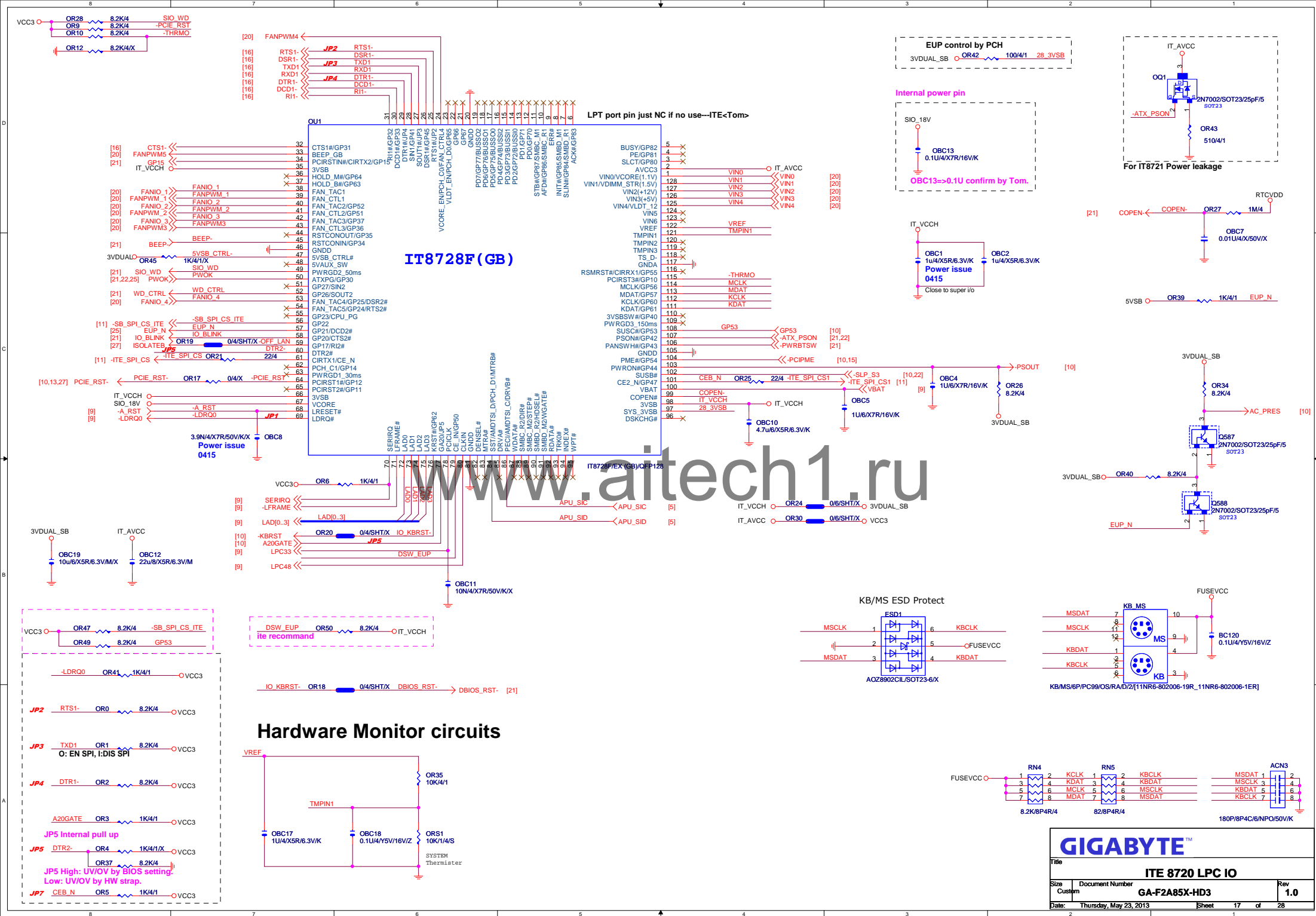


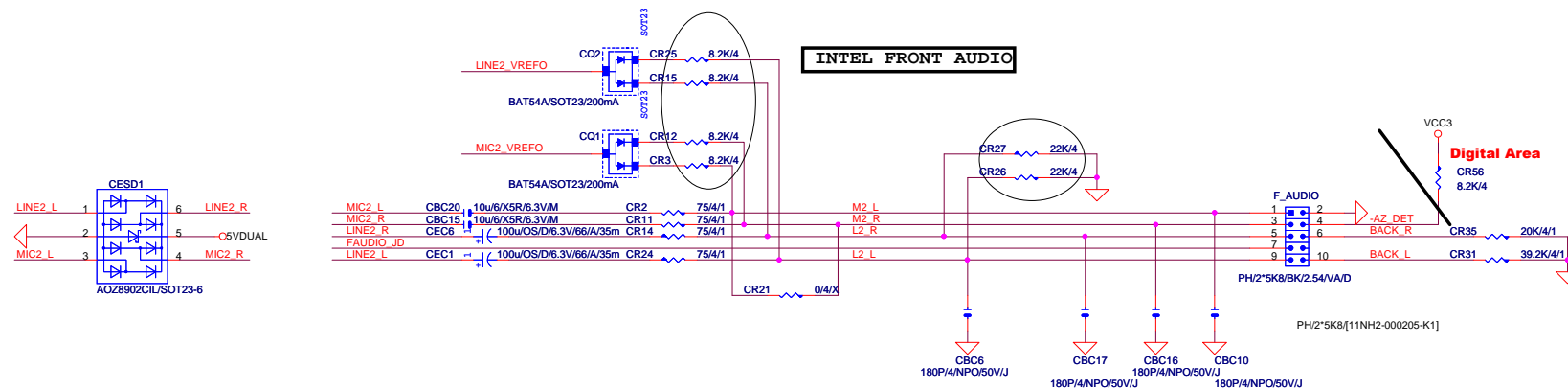
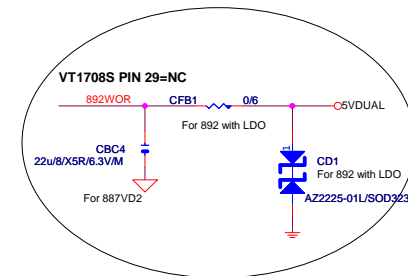


**PCI  
SLOT**

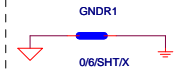




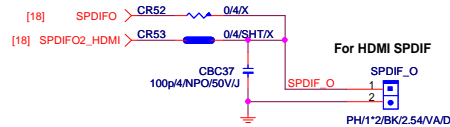




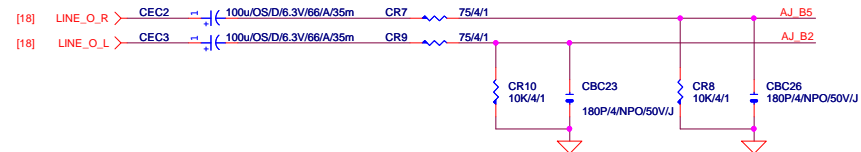
Between Audio to USB\_LAN



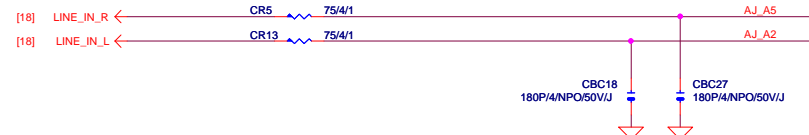
SPDIF



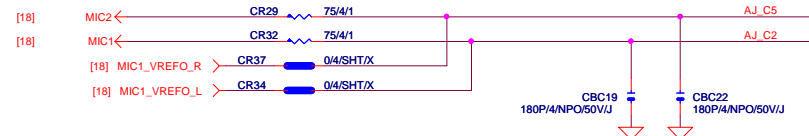
LINE OUT  
FRONT OUT



LINE-IN

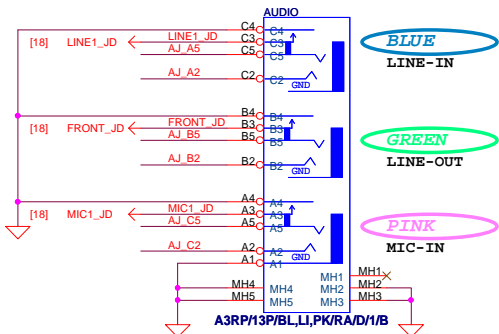
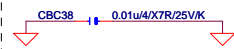


MIC



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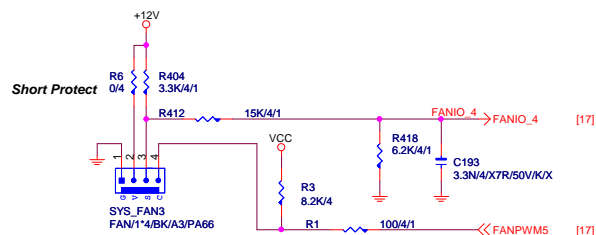
For Audio precision test



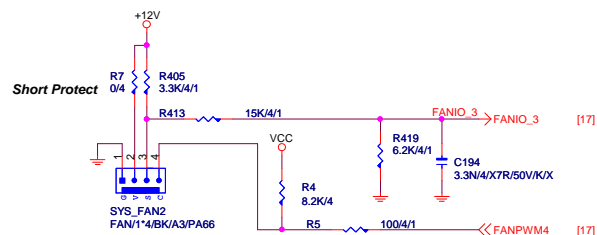
A3RP/13P/BL/LI/PK/RA/D/H/B  
A3RJ/13P/B/[11NR6-403006-01\_11NR6-403006-02]  
3RJ+15P/[11NR6-403004-11]

GIGABYTE™			
Title			
AUDIO JACK			
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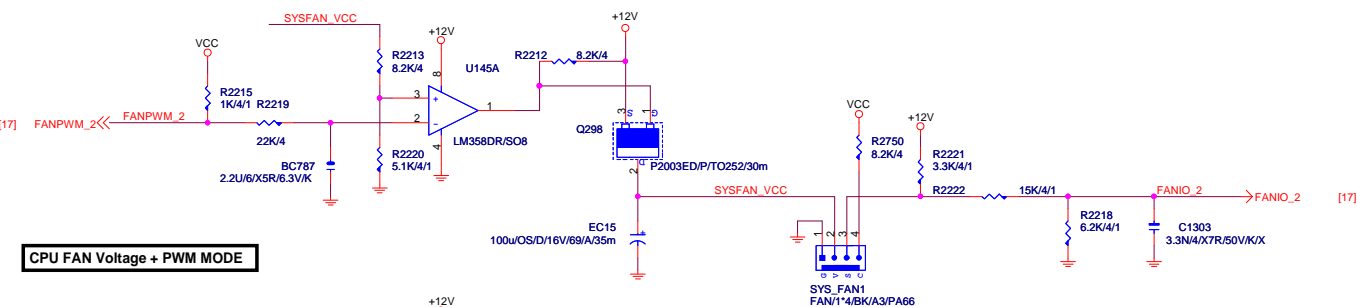
# SYSTEM FAN3 PWM MODE



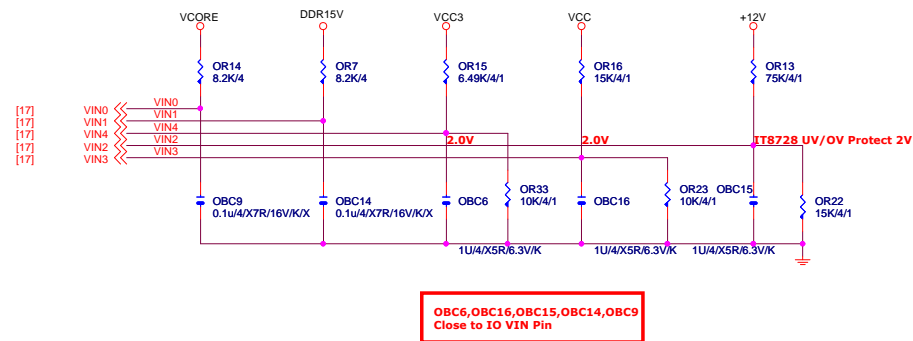
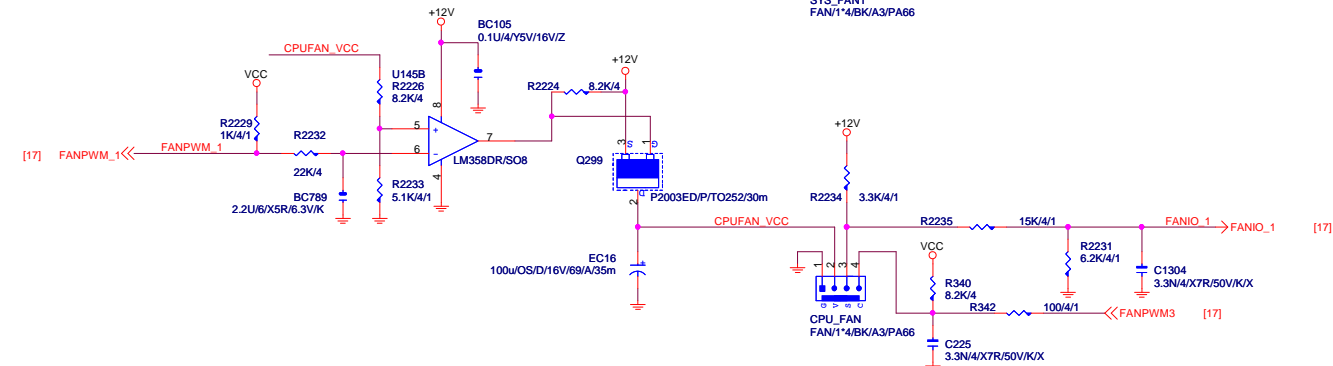
# SYSTEM FAN3 PWM MODE



# SYSTEM FAN1 Voltage Mode



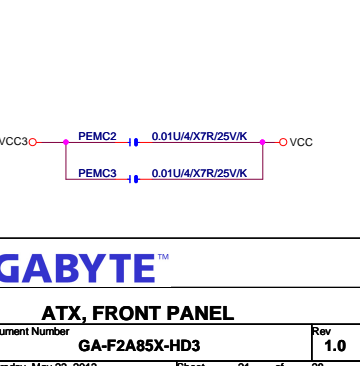
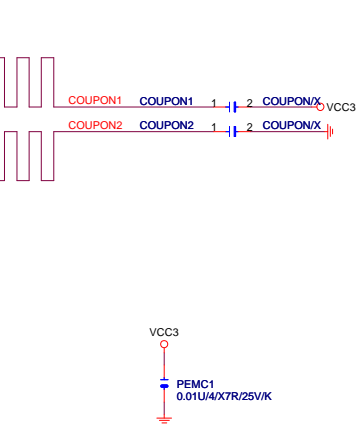
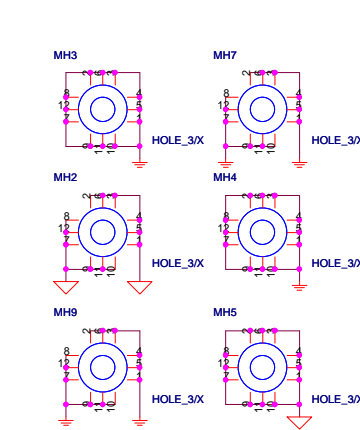
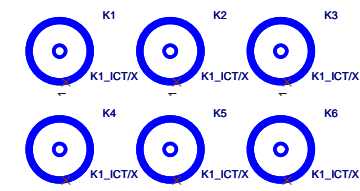
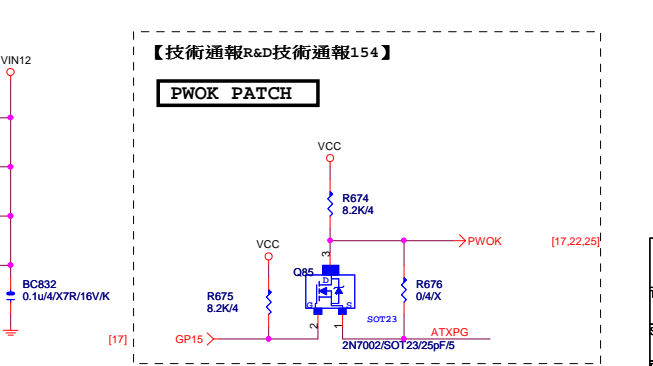
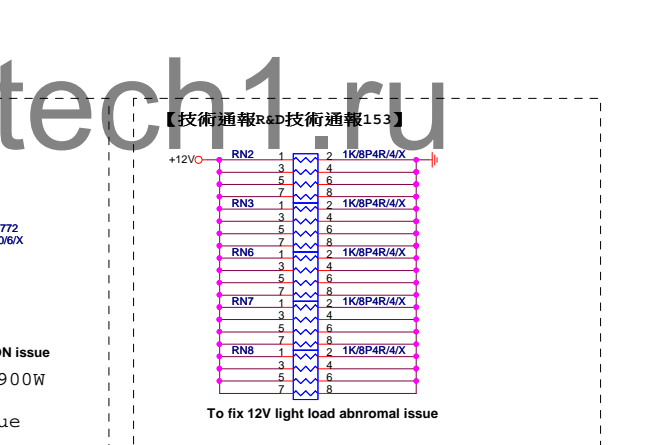
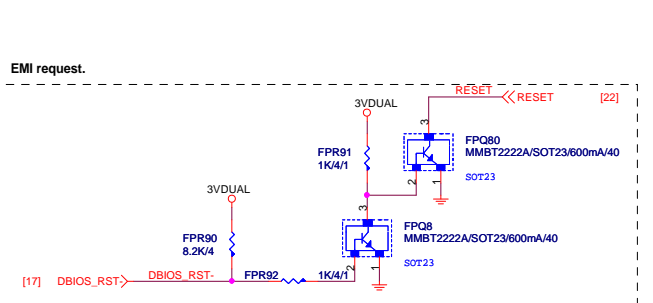
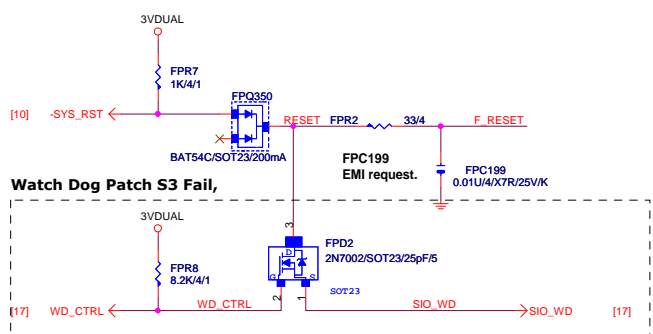
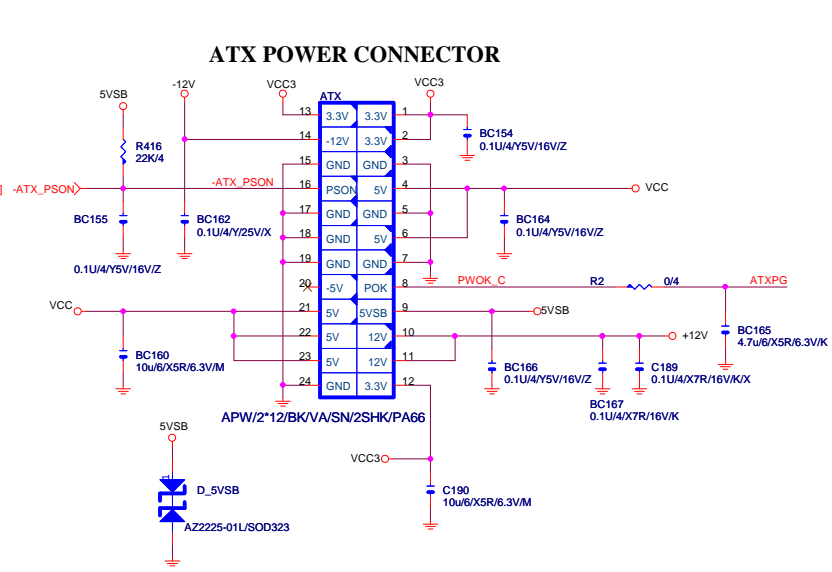
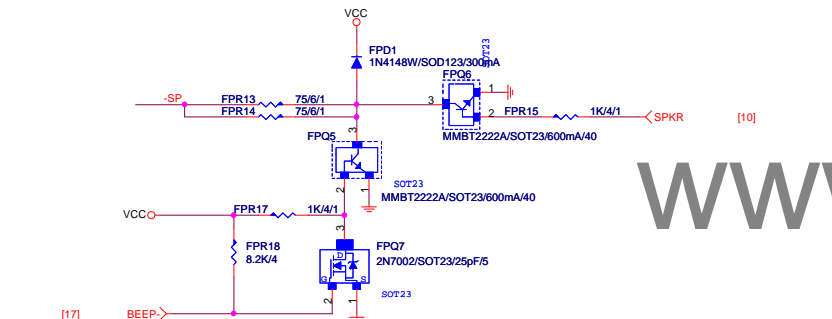
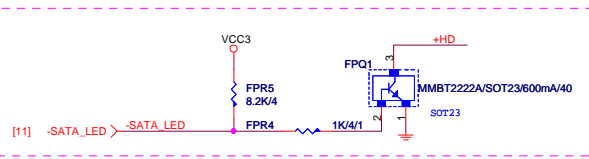
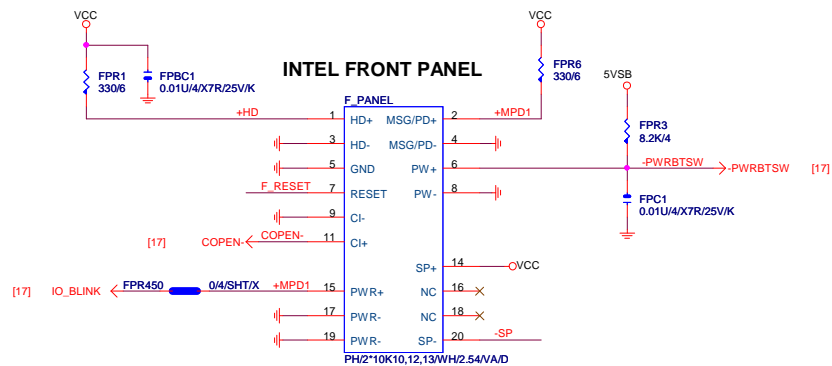
# CPU FAN Voltage + PWM MODE

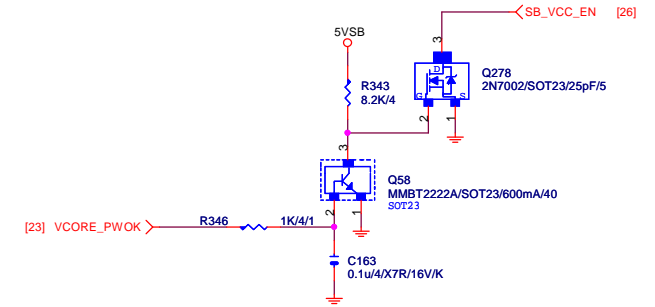
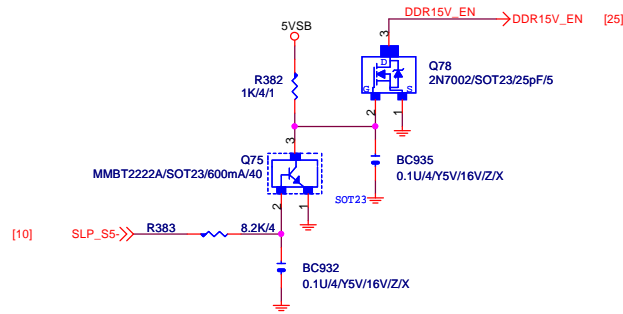
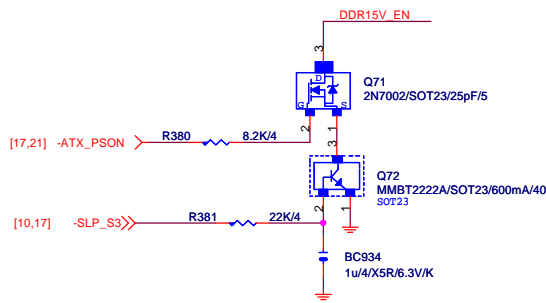


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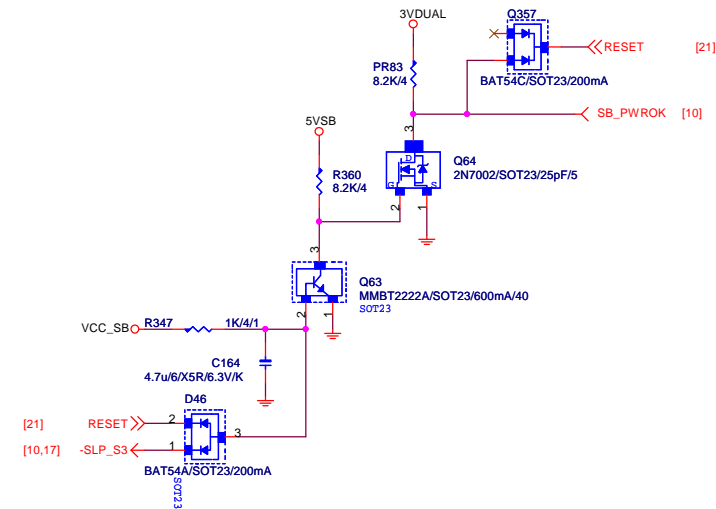
GIGABYTE™			
Title		FAN/HWMO	
Size	Document Number	Rev	
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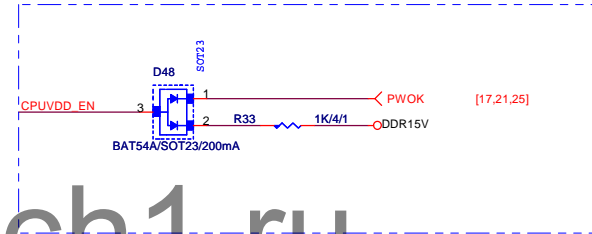


ADJ PWM\_EN Sequence, See Page 22 Red Frame  
Change DR23, DR30 ADJ LL Meet AMD Spec

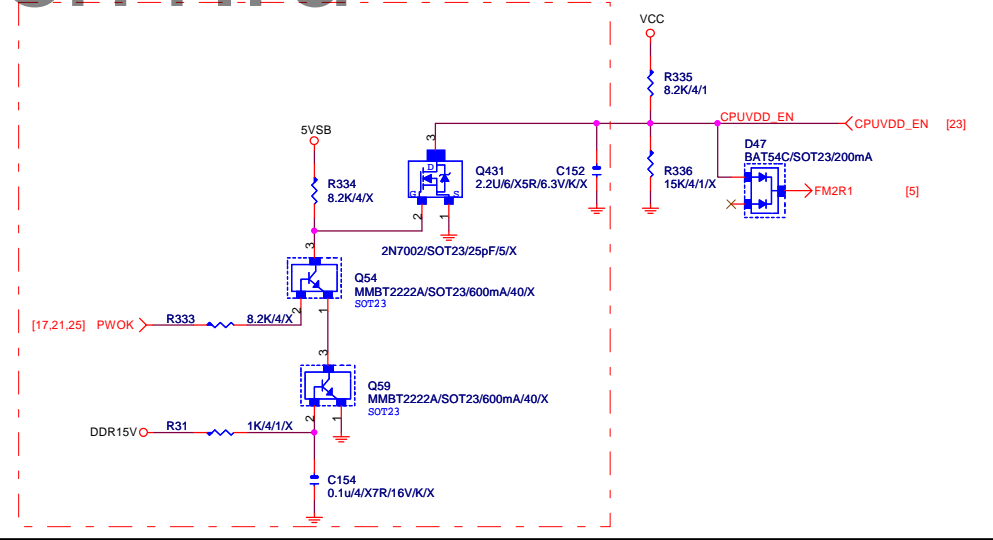


Colay

Rev : 1.0 pop



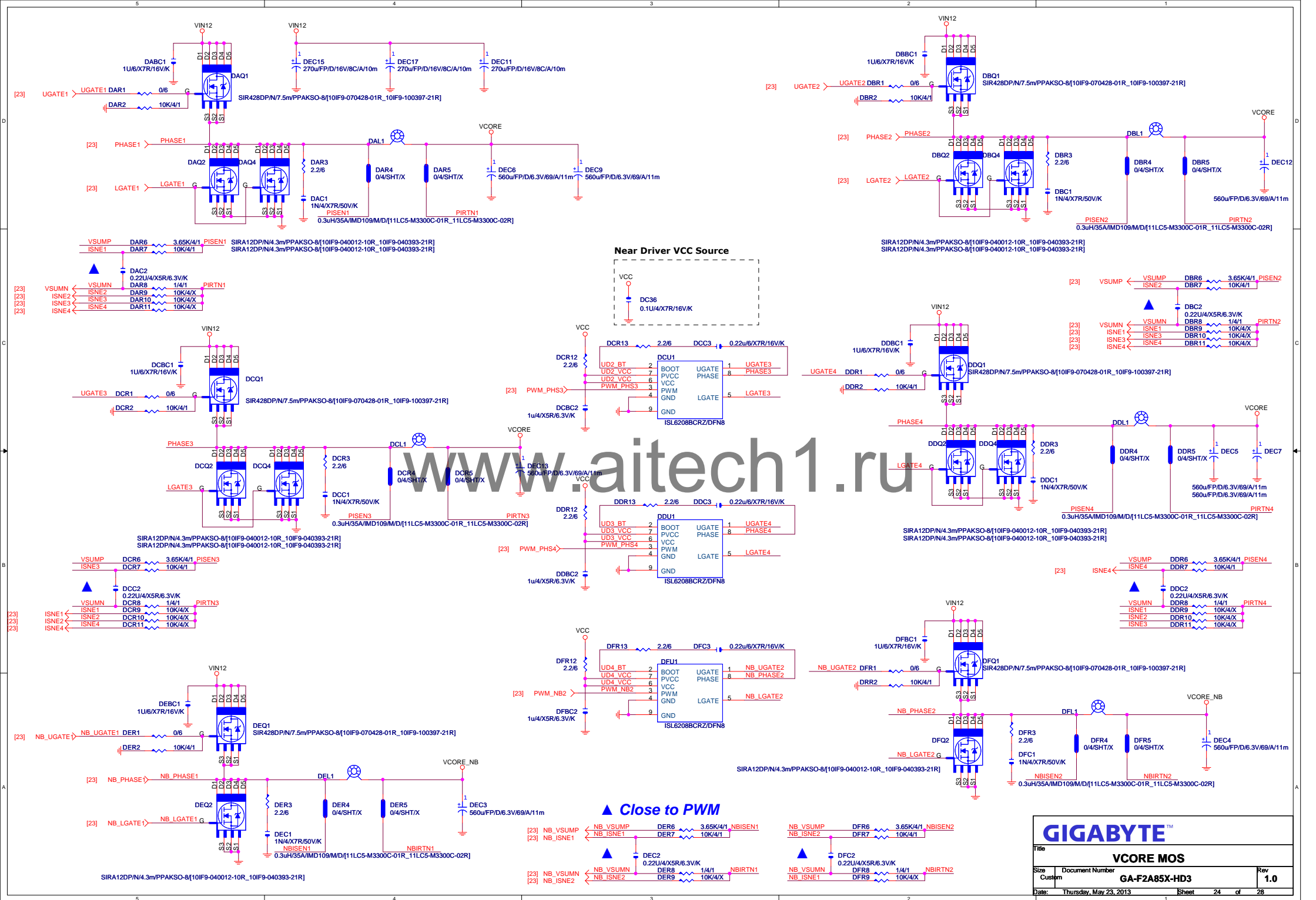
Rev: 0.1 pop



**GIGABYTE**™

Title			
POWER SEQUENCE			
Size	Document Number	Rev	
Custom	GA-F2A85X-HD3	1.0	
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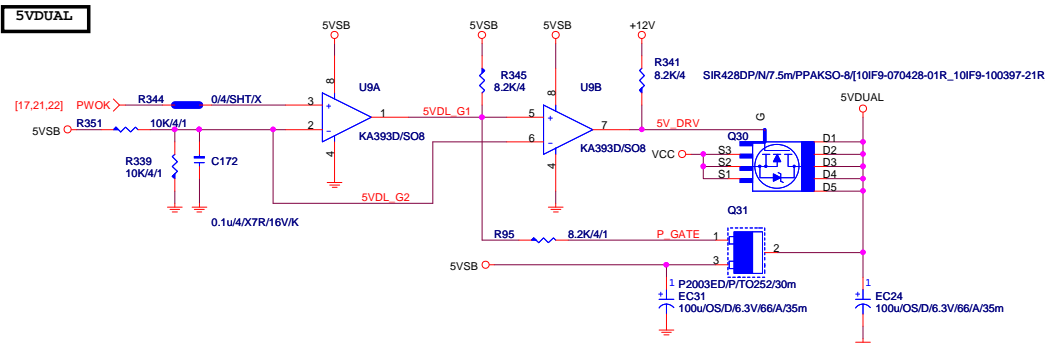




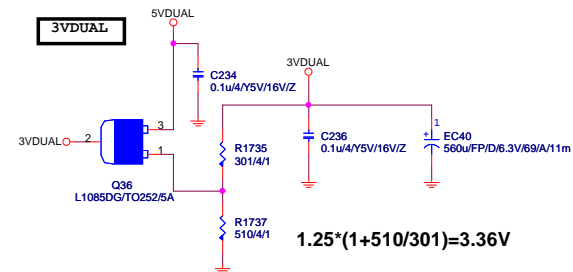
**GIGABYTE**

Title			<b>Vcore MOS</b>
Size	Document Number	Rev	
Custom	<b>GA-F2A85X-HD3</b>	<b>1.0</b>	
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# 5VDUAL

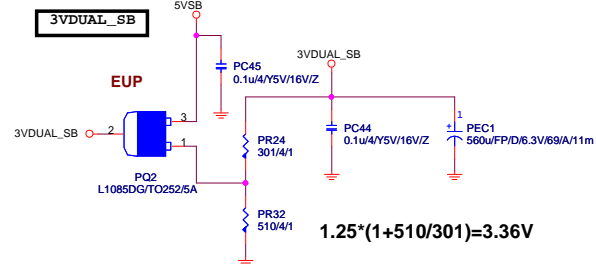


# 3VDUAL



$$1.25 \cdot (1 + 510/301) = 3.36V$$

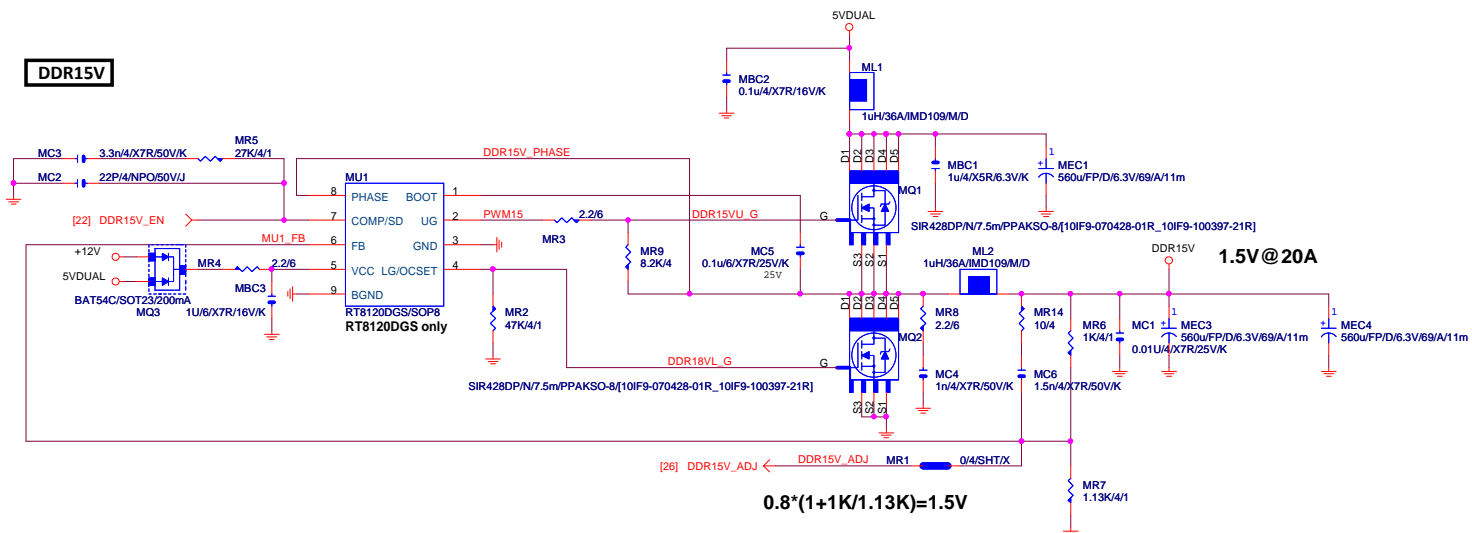
# 3VDUAL\_SB



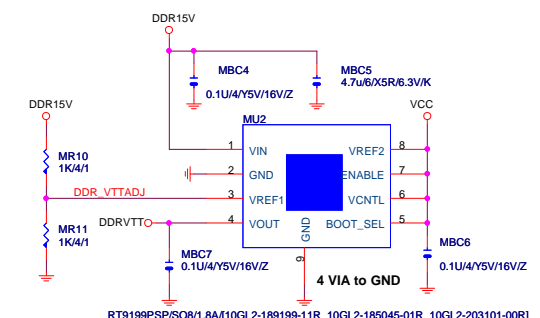
$$1.25 \cdot (1 + 510/301) = 3.36V$$

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# DDR15V



$$0.8 \cdot (1 + 1K/1.13K) = 1.5V$$

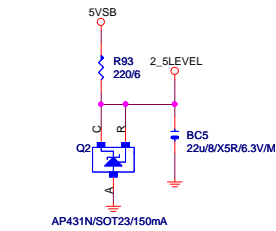


**GIGABYTE**

Title: **DDR POWER , VCC18**

Size: Custom Document Number: **GA-F2A85X-HD3** Rev: **1.0**

Date: Thursday, May 23, 2013 Sheet: 25 of 28

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Q62  
UP0111AMA5-00/SOT23-5/600mA[10GL4-067365-01R]

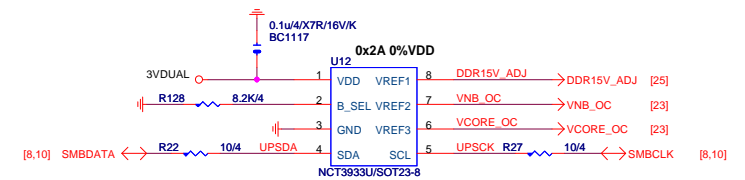
VCC3 1 VIN 5 VOUT 2 GND 3 EN 4 FB

R1 R394 2K/4/1 BC132 2.2u6/X5R/6.3V/K BC136 0.1uF/4Y5V/16V/Z BC18 22u8/X5R/6.3V/M

R2 R395 931/4/1 BC144 0.1uF/X7R/16V/K/X

EN>0.35V  
Vout=0.8\*(R1+R2)/R2

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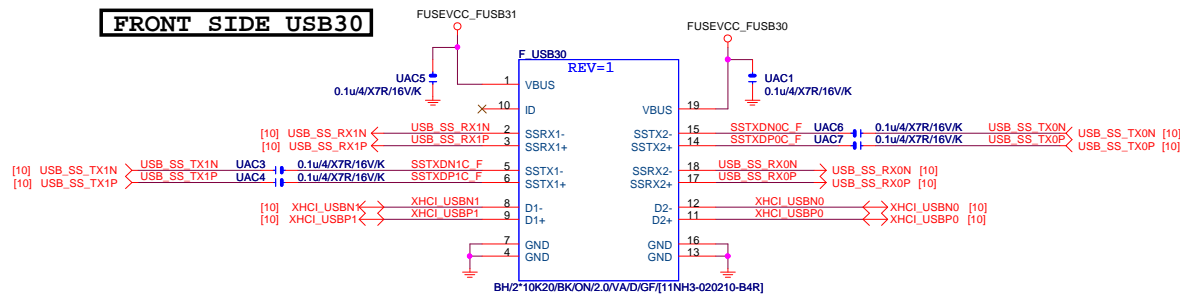


**GIGABYTE™**

Title			
VCC_SB&VCC11_DUAL/APU_VDD12, VDDA25			
Size	Document Number	Rev	
Custom	GA-F2A85X-HD3	1.0	
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# FRONT SIDE USB30



# REAR SIDE USB30

